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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/600,715 | 06/23/2003 | Vinod Sharma | 2207/861502 | 5754 |

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| EXAMINER |
|---|
| ELMORE, STEPHEN C |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2186 | |

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/600,715 | SHARMA, VINOD | |
| | Examiner | Art Unit | |
| | Stephen Elmore | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *13 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *26-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26,27,31,34,35,38,42 and 43* is/are rejected.

7)☒ Claim(s) *28-30,32,33,36,37,39-41 and 44* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

**DETAILED ACTION**

1. This Office action responds to the amendment, filed July 13, 2004, amending claims 34, 36 and 37.

2. Claims 26-44 remain for examination.

***Specification***

3. The objection to the specification is **withdrawn**.

***Claim Objections***

4. Claims 42-44 are objected to because of the following informalities:

   a. claim 42, "An system" is non-idiomatic English;

   b. claims 43 and 44 inherit the deficiencies of the independent claim from which they depend.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

5. The rejections under 35 USC 112, second paragraph, are **withdrawn**.

***Double Patenting***

6. The Terminal Disclaimer filed July 13, 2004 is approved. The obvious-type double patenting rejections are **withdrawn**.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 26, 27, 31, 34, 35, 38, 42 and 43 are rejected under 35 U.S.C. 102(e) as being anticipated by Boyd et al., US Patent 5,895,487.

Boyd teaches the claimed apparatus, merged tag array, system, and method, (claims 26, 31, 34, 38 and 42) as an integrated processor and L2 DRAM cache, see Abstract, Summary, and Figure 5, comprising:

**Claims 26 and 27,**

a. the limitations, a first data array, a second data array coupled to the first data array, and a merged tag array coupled to the second data array, wherein the merged tag array is to store directory information for the first data array and the second data array, are taught, see Figure 5, as the two L2 DRAM cache arrays belonging to integrated processors $51_1$ and $51_2$ (as the first and second data arrays), and the merged tag array is taught as global tag array 52 because it contains directory information of the two data arrays, since it has entries for each of the individual L2 caches, see col. 6, lines 11-19;

b. as to the limitation of claim 27, wherein the merged tag array is further coupled to a processor state control component, this limitation is taught as inherent to the teaching of a processor "PROC 1" being coupled to the first data array, because it is inherent that the processor's ability to change from one state to another be controlled by an included processor state control component;

**Claim 31,**

c. the limitations, a first directory field containing information about the contents of a corresponding set in a first data array, and a second directory field containing information

about the contents of a corresponding set in a second data array, are taught, see Figure 5 and col. 6, lines 11-19, as the entries TAG 1 (directory field 1) and TAG 2 (directory field 2) in the global tag array 52;

**Claims 34 and 35,**

d. the limitations, a first array to store data, and a second array to store data, wherein the second array is coupled to the first array, and a third array to store tags for both the first array and the second array, these are taught, see Figure 5, as the two L2 DRAM cache arrays belonging to integrated processors $51_1$ and $51_2$ (as the first and second data arrays), and the merged tag array is taught as global tag array 52 because it contains merged directory information of the two data arrays, since it includes tag entries for the contents of the data arrays of both of the individual L2 caches, see col. 6, lines 11-19;

e. as to claim 35, wherein a tag stored in the third array identifies the contents of a set in the first array and the second array, this limitation is taught, see Figure 5 and col. 6, lines 11-19, as the combination of the set of entries TAG 1 (directory field 1) and TAG 2 (directory field 2) in the global tag array 52;

**Claim 38,**

f. the claimed steps of, issuing a request for information to a first data array, a second data array, and a merged tag array, wherein the merged tag array stores directory information for

the first data array and the second data array; determining from the merged tag array whether the request generated a cache hit in the first data array or second data array; and providing information from the first data array or second data array based on the results of said

determination, these are taught, see Figure 5, as the two L2 DRAM cache arrays belonging to integrated processors $51_1$ and $51_2$ (as the first and second data arrays), and the merged tag array is taught as global tag array 52 because it contains directory information of the two data arrays, since it has entries for each of the individual L2 caches, see col. 6, lines 11-19, and the limitation of determining whether the request generated a cache hit in the first data array or second data array is further taught, see col. 6, lines 36, by the teaching "If there is a hit in the L2 tag array, continue";

**Claims 42 and 43,**

g. the following limitations are taught, see Figure 5, a central processing unit ("PROC 1");

a first data array coupled to the central processing unit ("DRAM L2"); a second data array coupled to the central processing unit and the first data array ("DRAM L2" associated with or integral with "PROC 2" which is coupled to the first data array "DRAM L2" associated with or integral with "PROC 1"); a merged tag array ("GLOBAL TAG - 52") coupled to the central processing unit and the second data array, wherein the merged tag array is to store directory information for the first data array and the second data array; and a system random access memory coupled to the merged tag array and the second data array (taught as the system random access memory coupled to the global tag 52 as shown in Figure 11, element 1121, as "Main Memory";

h. as to claim 43, wherein the central processing unit includes a processor state control component, this limitation is taught as inherent to the processor "PROC 1" because it is

inherent that the processor's ability to change from one state to another be controlled by an included processor state control component.

***Response to Arguments***

9. Applicant's arguments, filed July 13, 2004, with respect to the rejection(s)of claim(s) 26-37 under obvious-type double patenting and claims 34-37 under 35 USC 112, second paragraph, have been fully considered and are persuasive. Therefore, these rejections have been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art patent reference Boyd et al., US Patent 5,895,487.

***Allowable Subject Matter***

10. The previous indications of allowable subject matter are withdrawn due to the newly found prior art reference and rejections which have been applied thereupon.

11. Claims 28-30, 32, 33, 36, 37, 39-41, and 44 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Elmore whose telephone number is (703) 308-6256. The examiner can normally be reached on Mon-Fri from 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on (703) 305-3821. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stephen Elmore
Assistant Examiner
Art Unit 2186

August 3, 2004